ARTICLE 19 AMENDMENT

CLAIMS

1. (Amended) A PLL frequency synthesizer comprising:

a plurality of loop filters with different cutoff frequencies;

an oscillation section that generates a frequency signal corresponding to a voltage output from one of said plurality of loop filters;

a variable frequency fluctuation component elimination circuit that is provided between said oscillation section and an oscillation signal output terminal and that eliminates a frequency fluctuation component that varies for each of said plurality of loop filters; and

a control section that performs control of said frequency fluctuation component elimination circuit in accordance with switching of said loop filters.

2. The PLL frequency synthesizer according to claim 1, wherein said frequency fluctuation component elimination circuit comprises a variable capacitance capacitor whereby self-resonance is performed with different frequency fluctuation components.

3. The PLL frequency synthesizer according to claim 1, wherein said frequency fluctuation component

elimination circuit comprises a resonance circuit that resonates with different frequency fluctuation components.

4. The PLL frequency synthesizer according to claim 1, further comprising resistors provided between a junction point at which a signal line whereby output from said oscillation section is fed back branches from an output line of said oscillation section and said oscillation section, in said feedback signal line and an output line subsequent to said junction point respectively.

5. A radio communication apparatus comprising the PLL frequency synthesizer according to claim 1.